

WHAT IS CLAIMED IS:

1. A backplane, comprising:
 2. a front side portion having a plurality of front connector holes organized into a set of standardized front connector segments; and
 5. a rear side portion having a plurality of rear connector holes organized into a set of rear connector segments that substantially correspond to said front connector segments,
 9. wherein at least one rear connector segment includes a set of non-standard rear connector holes that are in addition to said at least one rear connector segment's rear connector holes organized into a standardized form such that said set of non-standard rear connector holes are operable to support a signal pathway independent of a standard bus path supported by at least one of said standardized front connector segments.

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1 2. The backplane as set forth in claim 1, wherein
2 said set of standardized front connector segments and
3 said set of rear connector segments comprise five
4 connector segments each, said connector segments
5 conforming to the Compact Peripheral Component
6 Interconnect (CPCI) standard.

1 3. The backplane as set forth in claim 1, wherein
2 said signal pathway supported by said set of non-standard
3 rear connector holes of said at least one rear connector
4 segment comprises a proprietary input/output (I/O) bus
5 system.

1 4. The backplane as set forth in claim 1, wherein
2 said front connector holes of said standardized front
3 connector segments and said rear connector holes of said
4 corresponding rear connector segments are coupled
5 together so as to form through-holes.

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1 5. The backplane as set forth in claim 1, wherein
2 said signal pathway supported by said set of non-standard
3 rear connector holes of said at least one rear connector
4 segment is operable to carry at least one user-defined
5 signal.

1 6. The backplane as set forth in claim 1, wherein
2 said set of standardized front connector segments and
3 said set of rear connector segments conform to one of the
4 VME and Eurocard standards.

1 7. The backplane as set forth in claim 1, wherein
2 said set of standardized front connector segments and
3 said set of rear connector segments conform to the
4 MultiBus standard.

1 8. The backplane as set forth in claim 1, wherein
2 said set of non-standard rear connector holes of said at
3 least one rear connector segment comprises at least one
4 column of connector holes.

1 9. A method for introducing user-defined signals
2 into a Compact Peripheral Component Interconnect (CPCI)-
3 compliant backplane, comprising the steps:

4 providing a front side portion of said
5 backplane with a plurality of front connector holes that
6 are organized into a set of standardized front connector
7 segments, wherein at least one of said standardized front
8 connector segments is operable to support a CPCI-
9 compliant bus for carrying CPCI signals; and

10 providing a rear side portion of said backplane
11 with a plurality of rear connector holes that are
12 organized into a set of rear connector segments which
13 substantially correspond to said front connector
14 segments, wherein at least one rear connector segment
15 includes a set of non-standard rear connector holes that
16 are in addition to said at least one rear connector
17 segment's rear connector holes organized into a
18 standardized form such that said set of non-standard rear
19 connector holes are operable to support a signal pathway
20 independent of said CPCI-compliant bus.

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1 10. The method for introducing user-defined signals
2 into a CPCI-compliant backplane as set forth in claim 9,
3 wherein said signal pathway supported by said set of non-
4 standard rear connector holes of said at least one rear
5 connector segment is operable to carry at least one user-
6 defined signal.

1 11. The method for introducing user-defined signals
2 into a CPCI-compliant backplane as set forth in claim 10,
3 said wherein at least one user-defined signal comprises
4 a Super Frame Indicator (SFI) signal operable to control
5 the operation of a telecommunications rack in which said
6 backplane is deployed.

1 12. The method for introducing user-defined signals
2 into a CPCI-compliant backplane as set forth in claim 10,
3 said at least one user-defined signal comprises an
4 Extended Alarm Signal (EAS) operable to carry a plurality
5 of alarms generated in the operation of a
6 telecommunications rack in which said backplane is
7 deployed.

1 13. A connector system, comprising:
2 a Compact Peripheral Component Interconnect
3 (CPCI)-compliant backplane having a plurality of slots,
4 each slot including five front side connector segments
5 (denoted herein as P1 through P5) and five rear side
6 connector segments (denoted herein as rP1 through rP5)
7 that substantially correspond to said front side
8 connector segments, wherein at least one of said P1 and
9 P2 connector segments is operable to support a CPCI-
10 compliant bus and further wherein at least one of said
11 rP1 and rP2 connector segments is provided with a set of
12 non-standard connector holes in addition to standard rear
13 connector holes;
14 a front side card coupled to said backplane at
15 a particular slot, said front side card operating to
16 carry a plurality of CPCI signals via said CPCI-compliant
17 bus formed to interconnect said P1 and P2 connector
18 segments of said slots; and
19 a rear side card coupled to said backplane at
20 said particular slot's rear side connector segments, said
21 rear side card operating to carry at least one user-
22 defined signal via a rear side backplane bus formed to
23 interconnect said non-standard connector holes of said
24 rP1 and rP2 connector segments of said slots.

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1 14. The connector system as set forth in claim 13,
2 wherein said at least one user-defined signal is provided
3 from said rear side card to said front side card via a
4 coupling between said P3 and rP3 connector segments.

1 15. The connector system as set forth in claim 13,
2 wherein said at least one user-defined signal is provided
3 from said rear side card to said front side card via a
4 coupling between said P4 and rP4 connector segments.

1 16. The connector system as set forth in claim 13,
2 wherein said at least one user-defined signal is provided
3 from said rear side card to said front side card via a
4 coupling between said P5 and rP5 connector segments.

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1 17. The connector system as set forth in claim 13,
2 wherein said at least one user-defined signal comprises
3 a Super Frame Indicator (SFI) signal operable to control
4 the operation of a telecommunications rack in which said
5 backplane is deployed.

1 18. The connector system as set forth in claim 13,
2 wherein said at least one user-defined signal comprises
3 an Extended Alarm Signal (EAS) operable to carry a
4 plurality of alarms generated in the operation of a
5 telecommunications rack in which said backplane is
6 deployed.

1 19. The connector system as set forth in claim 13,
2 wherein said P1 and P2 connector segments are formed as
3 a monoblock.

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1 20. The connector system as set forth in claim 13,
2 wherein said P4 and P5 connector segments are formed as
3 a monoblock.

1 21. The connector system as set forth in claim 13,
2 wherein said non-standard rear connector holes are
3 dimensioned to receive ultrashort press-in pins formed at
4 a corresponding connector portion of said rear side card.

1 22. A backplane, comprising:

2 a front side portion having a plurality of
3 front connector holes organized into a set of front
4 connector segments; and

5 a rear side portion having a plurality of rear
6 connector holes organized into a set of rear connector
7 segments that substantially correspond to said front
8 connector segments,

9 wherein at least one of said front connector
10 segments and said rear connector segments includes a set
11 of non-standard connector holes that are in addition to
12 standard connector holes forming said at least one
13 connector segment such that said set of non-standard
14 connector holes are operable to support a signal pathway
15 independent of a standard bus path supported by at least
16 one standard front connector segment.

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1 23. The backplane as set forth in claim 22, wherein
2 said set of front connector segments and said set of rear
3 connector segments comprise five connector segments each,
4 said connector segments conforming to the Compact
5 Peripheral Component Interconnect (CPCI) standard.

1 24. The backplane as set forth in claim 22, wherein
2 said signal pathway supported by said set of non-standard
3 rear connector holes of said at least one rear connector
4 segment comprises a proprietary input/output (I/O) bus
5 system.

1 25. The backplane as set forth in claim 22, wherein
2 said signal pathway supported by said set of non-standard
3 connector holes of said at least one of said front
4 connector segments and said rear connector segments is
5 operable to carry at least one user-defined signal.

1 26. The backplane as set forth in claim 22, wherein
2 said set of front connector segments and said set of rear
3 connector segments conform to one of the VME and Eurocard
4 standards.

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1 27. The backplane as set forth in claim 22, wherein
2 said set of front connector segments and said set of rear
3 connector segments conform to the MultiBus standard.

1 28. The backplane as set forth in claim 22, wherein
2 said set of non-standard connector holes of said at least
3 one of said front connector segments and said rear
4 connector segments comprises at least one column of
5 connector holes.

1 29. The backplane as set forth in claim 22, wherein
2 said set of non-standard connector holes of said at least
3 one of said front connector segments and said rear
4 connector segments are dimensioned to receive ultrashort
5 CPCI-compliant pins.